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Active Matrix Field Sequential Color Electrically Suppressed Helix Ferroelectric Liquid Crystal for High Resolution Displays

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Abstract:

In this article, we disclose a 3-inch 250ppi active matrix field sequential color electrically suppressed ferroelectric liquid crystal (ESHFLC) display. ESHFLC's ultra-fast response time (~10μs at 6.67V/μm) enables the display resolution to be tripled via field sequential color technique. Photo-alignment technology provides ESHFLC with optimal anchoring energy which contributes to a high contrast ratio over 10K:1. Specific 3T1C pixel circuit is designed to convert the analog signal to pulse width modulation. Thus the field sequential color ESHFLC display is achieved on LTPS TFT panel. With the delivered prototype, we successfully demonstrate the active matrix FSC ESHFLC integrated display system. We believe this display may replace IPS or FFS in the near future for portable mobile market. Moreover, high resolution FSC ESHFLC can find more applications in emerging virtual reality displays.

Author Keywords:

Ferroelectric Liquid Crystal Displays; Active Matrix Field Sequential Color; Virtual Reality; Fast Response

1. Introduction

Over the past several years, a novel electro-optical mode of ferroelectric liquid crystal named electrically suppressed helix ferroelectric liquid crystal (ESHFLC) has been discovered and developed by HKUST [1,2,3]. By controlling the anchoring energy comparable to but less than the elastic energy of the helix of ferroelectric liquid crystal (FLC), we can confine the FLC in the ESHFLC mode. ESHFLC mode has many advantages like chevron defects free, mechanical stability and high contrast ratio over conventional surface stabilized FLC. These advantages together with the inherent merits of FLC such as fast response (around 10 μs under 6.66V/μm), low driving voltage enable ESHFLC to be used in field sequential color displays [4]. The field sequential color can triple the current resolution thus ESHFLC has wide applications in emerging virtual reality and next generation liquid crystal displays.

2. ESHFLC Display Physical Background

The ESHFLC display mode is achieved by a few constrains. First, the pitch should be controlled just a few times less than the cell gap. Second, the anchoring energy plays an important role in the ESHFLC mode. It will affect the optical quality and electrical modulation. To control the anchoring energy, photo-alignment material azo-dye SD1 is utilized in fabrication. [5] Figure 1 shows the chemical formula for SD1.

In the absence of electric field, the ESHFLC takes on a two domain structure with two optical axis distributed with 2θ (FLC cone angle) in between. With the increasing of applied external electric field, the area of one domain will gradually increase and finally dominate the whole panel. Under a small electric field (1.66/μm), FLC helix finishes unwound process and all the molecules will be reoriented to the same position perpendicular to the electric field. As it is shown in the Figure 1, the molecules will switch between two states due to the polarity of the electric field. The inserted figure shows that the fast response time enables the ESHFLC saturates at an electric field with 3 kHz.

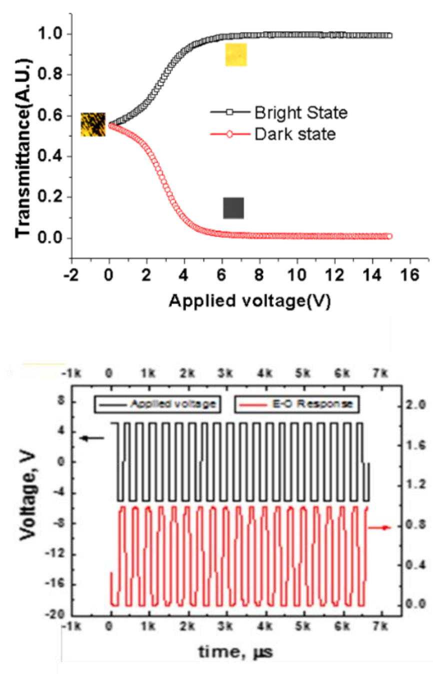

Figure 1: Transmittance voltage curve of ESHFLC, figure on the right is electro-optics performance of ESHFLC saturated at 3 kHz electric field with driven voltage 5V.

The response time for ESHFLC is fast due to the operation mechanism. Before ESHFLC helix unwound voltage, the response time is dependent on frequency because it is operating in the deformed helix ferroelectric liquid crystal region. After

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the helix unwounding process, FLC moves to the electric suppressed helix region and response time no longer relates to the frequency. With applied voltage 3.33V/ µm, response time can reach ~20 µs which is fast enough for field sequential color to avoid color breakup.

The color filter less display offers us several benefits: 3 times higher resolution; 3 times higher light efficiency; 3 times higher light efficiency; lower manufacturing cost for pattern color filters and etc.

3. Pixel Circuit Design for Active Matrix

Though enjoying several benefits for field sequential color display, ESHFLC still encounters certain issues when applied to the active matrix.

One problem is the binary switch (shown in Figure 2) is not compatible with the current Nematic LCD TFT array to generate gray level. We adopted pulse width modulation (PWM) method for ESHFLC on Silicon and reported in SID 2015. However, since the mobility of CMOS is several orders higher than amorphous or poly silicon, TFT on glass cannot provide sufficient high frame rate. Direct pulse width modulation is not going to work for ESHFLC. Herein, we designed a 3T1C pixel circuit (illustrated in Figure 2) for ESHFLC to generate gray scale in active matrix. [6]

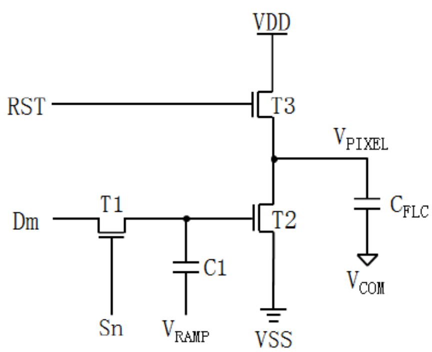

Figure 2: Proposed pixel circuit structure for AM ESHFLC to generate gray levels. (N type)

The proposed 3T1C pixel structure is used incorporating with a ramp signal. After all pixel are refreshed with corresponding data, the ramping signal starts, and together with the pixel circuit, they functioned as a pure voltage-to-PWM convector. The PWM output is coupled to the FLC electrode, hence, the grayscale is determined by the duration of on-off period. In such configuration, our driving scheme only have to scan the panel once, unlike the repeated scanning in bit-plane PWM method as mentioned above, this operation relax the speed requirement and make it suitable for thin-film transistor technology in direct-view display.

The beauty is that capacitor C1 would not response to AC signal (i.e. the V_{RAMP}), the amount of charge C1 holds during the frame is fixed and depended on D_m that initially fetched in during pixel addressing. As the same time, C_{FLC} is pre-charged to an initial voltage through T3. After that V_{RAMP} swing up, the gate of T2 follow the change. For different pixels, the initial voltage at the gate of T shift up or down depending on its pixel data. Namely that the gate of T2 is controlled by a data-depended ramping signal.

Now, we can see T2 is working under on-off mode (except for the short period from on to off transition). When VGS (T2) is above V_{TH} (T2), T2 is on; V_{GS} (T2) reach V_{TH}, T2 starts turning off and quickly V_{GS} (T2) swings below V_{TH} (T2), T2 is fully turned off. Therefore, the on-time duration is analog and linearly depended on data. Alternating the data voltage will effectively changing the On-Off ratio of the FLC state within the flame period, and this eventually generate gray levels in time domain perceived by human eyes.

Another problem is FLC is switched by spontaneous polarization current. Without sufficient spontaneous polarization charge provided to FLC material, the electro-optical performance will get deformed and result in gray scale inaccuracy. Thus, low temperaure poly silicon (LTPS) thin film transistors is adopted here for high operation current. The TFT array is fabricated by AU Optronics Corp.

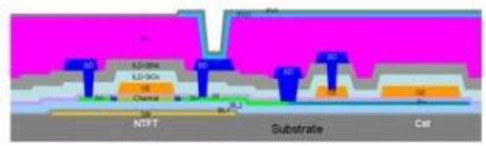

Figure 3: LTPS TFT cross section picture

4. Driving Scheme for Field Sequential Color and DC Compensation

Since ESHFLC performance is dependent on electric field polarity, we sacrifice half duration of frame time for DC compensation. Figure 4 shows the driving scheme for field sequential color ESHFLC. Frame rate is fixed at 60Hz while panel is addressed at 360Hz for field sequential and DC compensation. During the compensation time, the LED backlight is synchronously turned off to avoid gray level mess up. The panel one frame time (2.78ms) is also divided into two parts, data loading time and display time.

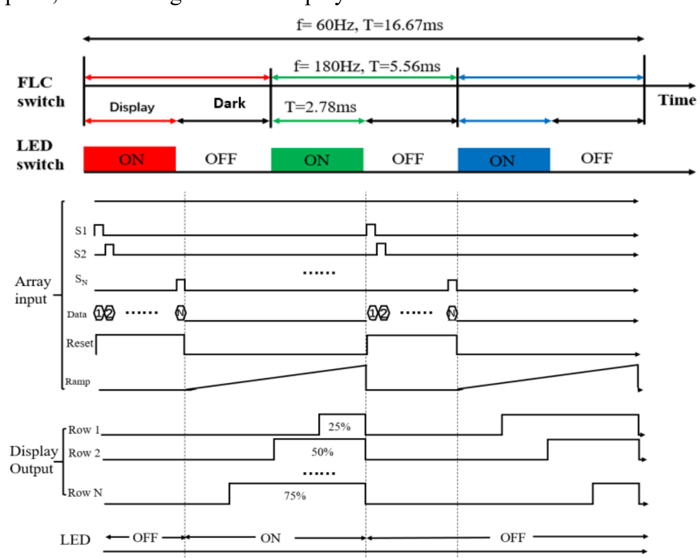

Figure 4: Driving scheme of Active Matrix FSC ESHFLC.

5. ESHFLC Prototype Development

We successfully demonstrate our active matrix field sequential color ESHFLC with RGB LED backlight and driving PCBs. The following images are showing good image quality and primary display color performances. The specifications of the prototype are shown in Table 1.

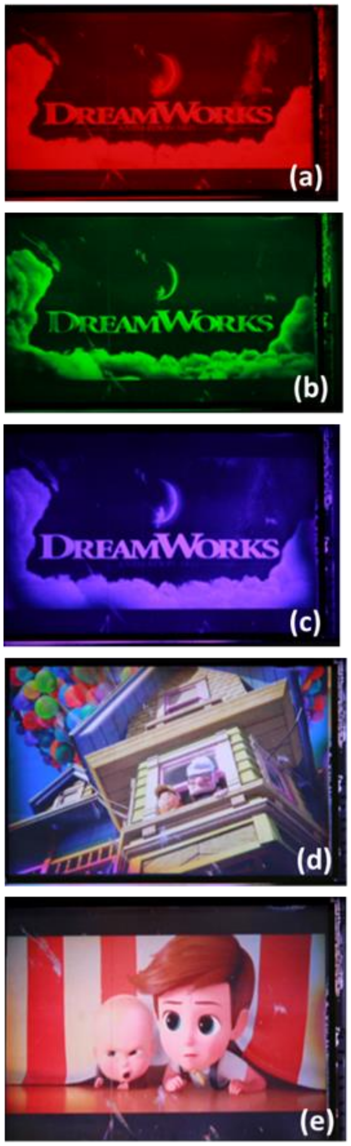

Figure 5: AM FSC ESHFLC display prototype (first three pictures show the R,G,B sub-frame image; the last two images show good color quality)

Display Diagonal	3”
Resolution	360 Gate x 640 Column
PPI	250 PPI
Pixel Pitch	102 um
Sub Frame Frequency	360 Hz

Table 1: AM FSC ESHFLC prototype specifications

6. Conclusion

To conclude, field sequential color ESHFLC with the advantages like low operation voltage, fast response time, high contrast ratio, wide viewing angle, is applied into active matrix TFT array flat panel displays for next generation high resolution portable displays and wide applications like virtual reality. Via 3T1C pixel design, we are able to generate 8 bit gray scale on LTPS TFT glass. Images and movies are demonstrated on the prototype to prove the concept.

Acknowledgement

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